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INTERNATIONAL CONFERENCE of SCIENTIFIC PAPER
AFASES 2015
Brasov, 28-30 May 2015

IMPROVEMENTS METHODS FOR DESIGN OF MULTIFUNCTIONAL REGISTERS WITH DECODED MODE SIGNALS

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Abstract: *This paper presents the research results regarding a comparison between two multifunctional registers types, with coded or decoded command validation signals. Also, the implementation costs, time parameters and the applicability in Finite State Machine - FSM synthesis are presented as conclusion.*

Keywords: *Multifunctional Registers, Moore Sequential System, Veitch – Karnaugh, Logic Gates, Truth Table, Priority Inputs Signals, FSM – Finite State Machine.*

1. INTRODUCTION

In this paper the authors continue the research of synthesis multifunctional registers, described in research papers [1],[2],[3]. The authors present in [1] the set of priority criteria orders for the multifunctional registers, denoted as RMF with the validation decode signals.

In this paper, the authors undertake a comparison between two multifunctional registers types, with the coded or decoded command validation signals. From this point of view, the authors analyze the implementation costs, time parameters and the applicability in FSM synthesis. The basic idea is to synthesis any digital systems using digital registers with multifunctional support. This means we use only the increment, parallel load, reset, decrement, shift signals. In this way, the system is costless which means optimal. This part of our design can be found inside a digital processor. The technology used is CMOS. The implementation cost represents the total number of the CMOS digital logic gates used. We assume that optimal design implementation means less digital circuit used compared with the already existing implementations, see [2],[3],[4].

2. MULTIFUNCTIONAL REGISTERS WITH DECODED MODE SIGNALS

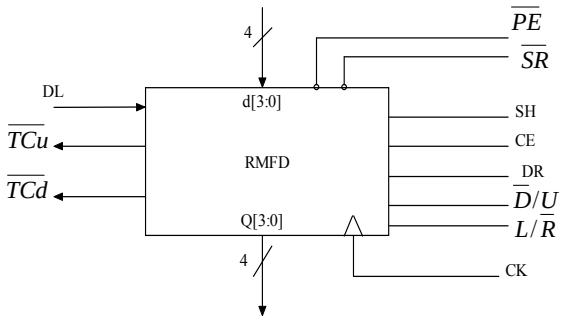

Figure 1 - RMF(decoded mode inputs)

Signals description:

Mode inputs: $\overline{SR}$ - Reset (High Priority), $\overline{PE}$ - Parallel Enable, SH – Logical

Shift($L/\overline{R}=0-Right$, $L/\overline{R}=1$-Left), CE – Count Enable(Low Priority) ($U/\overline{D}=0\rightarrow Down, U/\overline{D}=1\rightarrow UP$)

Data: d[3:0] – input data in parallel load mode, Q[3:0] –output data, DR,DL – serial input data, left shift, right shift, $\overline{TC_u}$ - Terminal Count Up (Q[3:0]=1111, last state), $\overline{TC_D}$ - Terminal Count Down (Q[3:0]=0000, last state).

CK – clock input, active on positive edge signal.

The functional behavior is described in Table 1.

Mode	$\overline{SR}\ \overline{PE}$ SH CE $L/\overline{R}$ $U/\overline{D}$ CK	$Q[3:0]_{n+1}$
Hold	1 1 0 0 - -	$Q[3:0]_n$
Reset	0 - - - - - ↑	0000
Parallel Load	1 0 - - - - ↑	$d[3:0]_n$
Shift Right	1 1 1 - 0 - ↑	$DRQ[3:1]_n$
Shift Left	1 1 1 - 1 - ↑	$Q[2:0]_n DL$
Count Down	1 1 0 1 - 0 ↑	$[Q_n-1]_n$ mod
Count UP	1 1 0 1 - 1 ↑	$[Q_n+1]_n$ mo

Table1 – RMF functionality

Observation: From paper [1], we consider only 4 bits for input/output data. This limitation doesn't affect the presented research idea.

Based on functionality modes and priority orders, we deduced the following equations (Di- data inputs on flip-flop D, Qi- outputs from flip-flop D).

$$D_i=\overline{SR}\cdot(PE\cdot d_i+\overline{PE}\cdot(SH\cdot(\overline{L/\overline{R}\cdot Q_{i+1}+L/\overline{R}\cdot Q_{i-1}})+\overline{SH}\cdot(CE\cdot(\overline{U/\overline{D}\cdot(\overline{Q_i}\oplus\varphi_i)+U/\overline{D}\cdot(Q_i\oplus\psi_i)})+\overline{CE}\cdot Q_i)))$$

$$D_3=\overline{SR}\cdot(PE\cdot d_3+\overline{PE}\cdot(SH\cdot(\overline{L/\overline{R}\cdot DL+L/\overline{R}\cdot Q_2})+\overline{SH}\cdot(CE\cdot(\overline{U/\overline{D}\cdot(\overline{Q_3}\oplus\varphi_3)+U/\overline{D}\cdot(Q_3\oplus\psi_3)})+\overline{CE}\cdot Q_3)))$$

$$D_0=\overline{SR}\cdot(PE\cdot d_0+\overline{PE}\cdot(SH\cdot(\overline{L/\overline{R}\cdot Q_1+L/\overline{R}\cdot DR})+\overline{SH}\cdot(CE\cdot(\overline{U/\overline{D}\cdot(\overline{Q_0}\oplus\varphi_0)+U/\overline{D}\cdot(Q_0\oplus\psi_0)})+\overline{CE}\cdot Q_0)))$$

where $i\in\{1,2\}$ and φ_i,ψ_i represent the "i^{th}" rank function for the down- or adder binary counter.

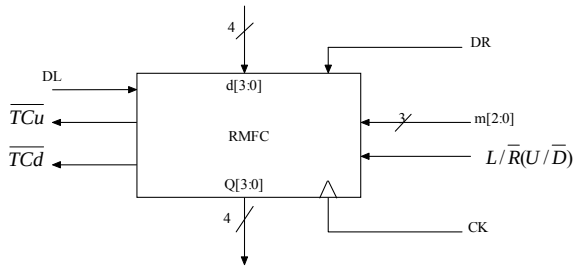

Figure 2 – RMFC design

$$\varphi_i=\prod_{k=0}^{i-1}\overline{Q_k}\ ,\ \psi_i=\prod_{k=0}^{i-1}Q_k$$

or

$$\varphi_i=\varphi_{i-1}\cdot\overline{Q_{i-1}}\ ,\qquad \psi_i=\psi_{i-1}\cdot Q_{i-1}\qquad \text{and}\qquad \varphi_0=\psi_0=1$$

We used a MUX2x1, described in figure 3, [1].

Taking into consideration the dynamic parameters for the digital circuits, like propagation delay times, set up times, hold times, one obtains the minimum expression for the clock period (equation (8) in [1]).

$$\underline{T_i}=\underline{t_{s\_u}}(D)+\overline{t_b}+\overline{t_p}(\varphi_i,\psi_i)+\overline{t_p}(86)+4\overline{t_p}(MUX)=$$

$$=\underline{t_{s\_u}}(D)+\overline{t_b}+i\cdot\overline{t_p}(08)+\overline{t_p}(86)+4\overline{t_p}(MUX)=230n\sec$$

or $\overline{f_1}=4{,}35MHz$ (2)

In the same paper [1], we calculated the same maximum clock parameters $(\overline{T},\overline{f})$ for another priority order criteria when the best values were obtained.

So, the conclusion from [1] is that dynamic parameters depends on the priorities allocation modes.

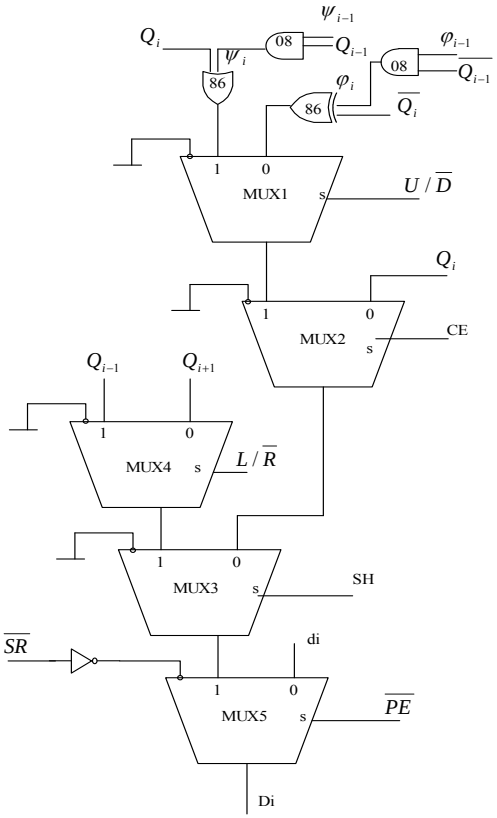

Figure 3 – RMF digital implementation

3. SYNTHESIS FOR THE SEQUENTIAL SYSTEM USING RMF WITH DECODED MODE SIGNALS

The unused mode or data inputs are disabled by connection to ground (0 logic). The truth table was completed as: if priority command signal is activated, the next low priority signals are *x* (0 or 1 logic)

$U/\overline{D}$ has 0 logic value for the DEC mode and 1 logic value for INC mode in the Hold state, the commands are disabled

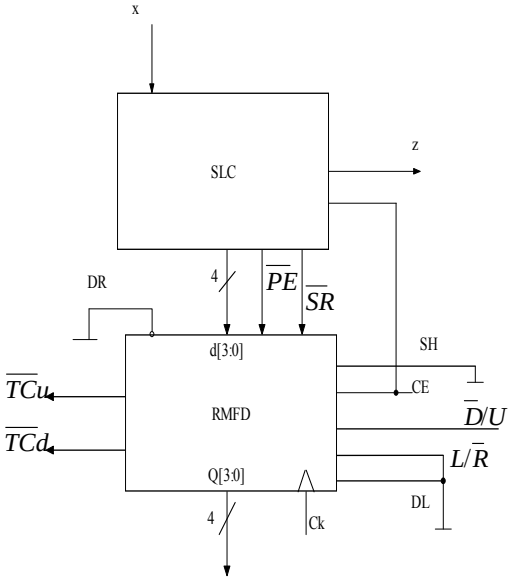

Figure 4 - Automata implementation architecture with RMFD

Considering the (1) priority order ($\overline{SR}$ - High Priority, SH – Low Priority), using Tables 2, results the next truth table, figure 5.

X / $Q_2Q_1Q_0$	$Q[2:0]_{n+1}$		$\overline{SR}$		$\overline{PE}$		CE		Z
000	001	101	1	1	1	0	1	-	0
001	010	110	1	1	1	0	1	-	0
011	001	100	1	1	0	1	-	1	1
010	001	011	1	1	1	1	1	1	1
110	010	100	1	1	0	0	-	-	0
111	000	000	0	0	-	-	-	-	0
101	001	100	1	1	0	1	-	1	0
100	100	100	1	1	1	1	0	0	0

Table 2

	d_2		d_1		d_0			
$U/\overline{D}$ / X / $Q_2Q_1Q_0$	0	1	0	1	0	1	0	1
000	-	1	-	0	-	1	1	-
001	-	1	-	1	-	0	1	-
011	0	-	0	-	1	-	-	1
010	-	-	-	-	-	-	0	1
110	0	1	1	0	0	0	-	-
111	-	-	-	-	-	-	-	-
101	0	-	0	-	1	-	-	0
100	-	-	-	-	-	-	-	-

Figure 5 – Truth Table

Using the Veitch-Karnaugh method, results the following equations:

$$\overline{SR} = \overline{Q_2}\,\overline{Q_1}\,\overline{Q_0}$$

$$\overline{PE} = \overline{\bar{x}\cdot[Q_1Q_0 + Q_2Q_1 + Q_0Q_2] + x\cdot(Q_2 \oplus \overline{Q_1})}$$

$$CE = \overline{Q_2\,\overline{Q_0}\cdot\overline{Q_1}}$$

$$\overline{D}/U = \overline{\bar{x}\cdot Q_1 + xQ_2}$$

$$Z = \overline{Q_2}Q_1$$

$$d_3 = 0$$

$$d_2 = x\cdot\overline{Q_0}$$

$$d_1 = \overline{Q_0} \oplus x$$

$$d_0 = \bar{x}\cdot Q_0 + x\cdot\overline{Q_2}\,\overline{Q_0}$$

(3)

If the SLC system would be implemented with logic gates as: AND (2 inputs), OR(2 inputs), XOR(2 inputs), NAND(2 inputs), 23 elementary circuits will be obtained, $C_{dec} = 23$.

4. SYNTHESIS OF SEQUENTIAL SYSTEM USING RMF WITH CODED MODE SIGNALS (RMFC)

If we consider the same Moore automata, we use only the Hold, Reset, INC/DEC, Parallel Load functions as:

- $m_2 \equiv 0$ (use only 2 codify bits)
- DL=DR=0 (the Shift function isn't used)
- $d_3 = 0$ (the automaton has only 8 states)

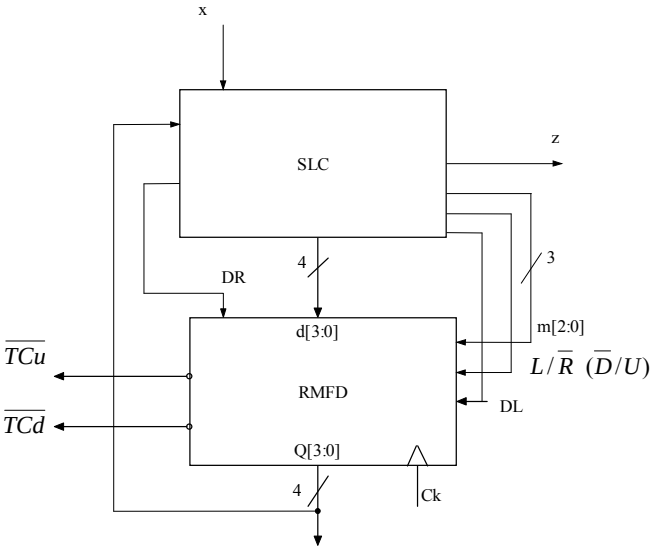

Figure 6 - Architecture of automata implemented with RMFC

The codifying function is defined in Table 3.

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$m_2m_1m_0$	Mode	$L/\overline{R}(U/\overline{D})$
000	HOLD	-
001	Reset	-
010	Paralle l Load	-
011	Count Up	1
011	Count Down	0

Table 3 – Mode Coding

The proposed system use only one RMFC and SLC which generates the output *z* signals, m[2:0], $L/\overline{R}(U/\overline{D})$.

The RMFC implementation became the one illustrated in Table 4.

	$Q[2:0]_{n+1}$				
m_1m_0 / X / $Q_2Q_1Q_0$	0	1	0	1	-
	Z				
000	001	101	011	010	0
001	010	010	011	010	0
011	001	100	010	011	1
010	001	011	010	011	1
110	010	100	010	010	0
111	000	000	001	001	0
101	001	100	010	010	0
100	100	100	000	000	0

$L/\overline{R}(U/\overline{D})$ d_2 d_1
d_0

X / $Q_2Q_1Q_0$	0	1	0	1	0	1	0	1
000	1	-	-	1	-	0	-	1
001	1	-	-	1	-	1	-	0
011	-	1	0	-	0	-	1	-
010	0	1	-	-	-	-	-	-
110	-	-	0	1	1	0	0	0
111	-	-	-	-	-	-	-	-
101	-	0	0	-	0	-	1	-
100	-	-	-	-	-	-	-	-

Table 4 – State transition matrix

Using one of the synthesis methods (Veitch-Karnaugh, Quine-McCluskey), we obtain the following equations:

$$m_1 = \overline{Q_2} + Q_1 \oplus Q_0$$

$$m_0 = \overline{Q_2} \cdot (x \oplus \overline{Q_1}) + x \cdot Q_2 Q_0 + Q_1 \cdot (Q_2 \oplus \overline{Q_0})$$

$$z = \overline{Q_2} Q_1$$

$$U/\overline{D} = x \oplus \overline{Q_1}$$

$$d_2 = x \cdot \overline{Q_0}$$

$$d_1 = x \oplus \overline{Q_0}$$

$$d_0 = \overline{x} Q_0 + x \overline{Q_1} \cdot \overline{Q_0}$$

- .

If the above equations are implemented with the same elementary circuits, results costs C=18.

3. CONCLUSIONS & ACKNOWLEDGMENT

In this paper, the authors made a comparison between the 2 types of RMF: RMFD – Multifunctional Registers with validation signals of decoded commands and RMFC – Multifunctional Registers with coded mode signals.

The authors, already presented RMFD in [1] and the conclusion is that the maximum frequencies depends on the priority allocation order for the mode signals. In general, from our simulations, we can affirm that maximum allowed frequency is 5MHz.

From the comparison of 2 multifunctional register types, RMFD and RMFC results: RMFC allows a maximum frequency (lower than RMFD) but a cost greater than RMFD (See Tables 4 and 5, for the 2 modes of priorities assignments).

In section 3, the authors synthesized a Moore automata and proposed an original contribution to the states coding, taking into account that the most used RMF functions must be used most often (INC/DEC most often and Parallel Load as little).

The logical structure (SL) will contain less elementary circuits for the RMFC implementation as compared with RMFD, so there is cost compensation (RMFC more expensive than RMFD).

To design automation with separate inputs, which can be activated simultaneously, it is necessary to use RMFD.

Synthesis method	Implementation Costs (number of logic gates)	Clock frequency
RMFC	18	5 Mhz
RMFD	23	4.35Mhz

REFERENCES

[1] Al. Valachi, M. Timis, B. Aignatoaie, S. Tarcau, "Orders Priorities Settings Criteria for Multifunctional Registers," Electronics and Electrical Engineering ISSN 1392 – 1215, T 120, System Engineering, Computer Technology, The 14th International Conference ELECTRONICS'2010 Kaunas and Vilnius University – Lituania,

http://www.ee.ktu.lt/page.php?227 - T120, page.87.

[2] Drane, Theo, Cheung, Wai-chuen, Constantinides, G. "Correctly rounded constant integer division via multiply-add", in Circuits and Systems (ISCAS), 2012 IEEE International Symposium on Circuits and Systems, Seul - Korea, May 2012, pages 1243 – 1246.

[3] C. H. Roth, Fundamentals of Logic Design, West Publishing Company, 1999.

[4] Al. Valachi, R.Silion, M. Timis, “Improvement of FSM Synthesis using MSI and LSI Circuits,” Advances in Electrical and Computer Engineering. Academy of Technical Sciences of Romania, “Stefan cel Mare” University of Suceava, vol 5(12), no.1/23, 2005.

[5] Shepherd, B.J., "Right Shift for Low-Cost Multiply and Divide", in IEEE Transactions on Computer Arithmetic (Volume:C-20 , Issue: 12), august 2006, pages 1586 – 1589.

[6] Oberman, S.F., Flynn, M., "Division algorithms and implementations", in IEEE Transactions on Computer Arithmetic (Volume:46, Issue: 8) Comput. Syst. Lab., Stanford Univ., CA, USA, august 2002, pages 833 – 854.

[7] Lin Yuan, Gang Qu, Villa, T., Sangiovanni-Vincentelli,A., "An FSM Reengineering Approach to Sequential Circuit Synthesis by State Splitting", in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems(Volume:27,Issue: 6), may 2008, pages 1159 – 1164.

[8] M.Timis, A.Valachi, P.Cascaval, R.Silion, “A Comparison between Coded-Decoded Mode Signals on Multifunctional Registers“, 12th International Conference on Development and Application Systems, Suceava, Romania, 2014.