ASPECTS ABOUT FREQUENCY SYNTHESIZERS

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Abstract:*The communications systems objectives consist of maintaining communication depending on different facts like: cruising speeds, subscriber growth, efficient use of the allocated spectrum, expanding geographical coverage, possibility of reconfiguration depending on traffic density, provide new services and achieving affordable costs.*

In this context, effective management of the electromagnetic spectrum has led to the emergence of specific structures capable of stability to disturbance, flexibility and capacity development. These structures, which permit the production of highly stable frequency signal is called frequency synthesizers.The role of frequency synthesizers is very important, it represents the core and customary in transmitting and receiving equipment.

Frequency synthesizers reprezent that class of electronic circuit capable of generating one or more stable frequencies from one or more reference frequencies. The stability of the output frequency is at least equal with the reference frequency.There are two main conventional types of achieving phase/frequency synchronization of the output signal with the reference signal:PLL (phase locked loop) – consist in transfering stability of a highly stable component to a less stable element. Has quite large spectral purity, reproduce with high fidelity a reference signal scaled over a wide frequency range.DDS (direct digital synthesis) - good resolution, low switching times, opportunities for implementing digital modulations,

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1. INTRODUCTION TO FREQUENCY SYNTHESIZERS

Frequency synthesizer represent the class of electrical circuits capable of generating one or morefrequencies high stability, starting from one or more reference frequencies (fig. 1). Output frequencies stability is at least equal or higher than the input frequency f_0.

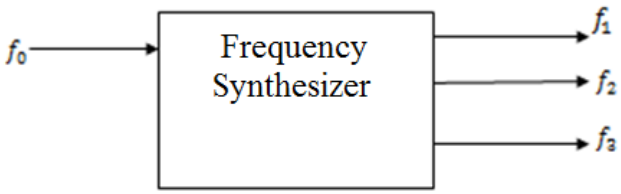


FIG 1. Block diagram of a frequency synthesizer.

Ideally is to obtain from one synthesizer a noise-free sine wave. Actually, this thing never happens, the output signal being affected in some measure by the presence of unwanted disruptive components.

The formula of a pure sine wave is:

$$V(t) = (V_0\ sin(2\pi f_0), \quad (1)$$

If we consider the amplitude fluctuationand the signal's phase, the formula will become:

$$V(t) = (V_0 + v(t))sin(2\pi f_0 t + \phi(t)), \quad (2)$$

where v(t) is the amplitude fluctuation, respectively ϕ(t) fluctuation of the phase.

When designing a frequency synthesizerit is envisaged that it meet certain main features:

-synthesized frequency range signal using a specific portion of the spectrum;

-network spread - the difference between two neighboring frequencies;

-spectral purity of the generated signal - signal to noise ratio is as high as possible;

-switching speed - speed that is reached at a frequency other;

- the number of frequencies generated - fully frequencies depending on the range and the difference;

-the possibility of performing different types of modulation amplitude, modulation in frequency or phase;

-continuity of the phase - phase synchronization maintaining;

-stability of frequency and amplitude output signal - this should not fluctuate greatly, as synthesized signal is lost;

-constructive features - features of some components of a frequency synthesizer;

-power consumption - power in watts of the frequency synthesizer;

-the cost.

2. METHODS OF FREQUENCI SYNTHESIS

PLL Synthesis

A frequency synthesizer using indirect PLL synthesis is based on a circuit that follows and faithfully reproduce a reference signal scaled over a wide frequency.

Frequency synthesizers using method horseback PLL phase generates the desired signal frequency with high enough spectral purity, and also, allows digital output frequency according with specified frequency output.

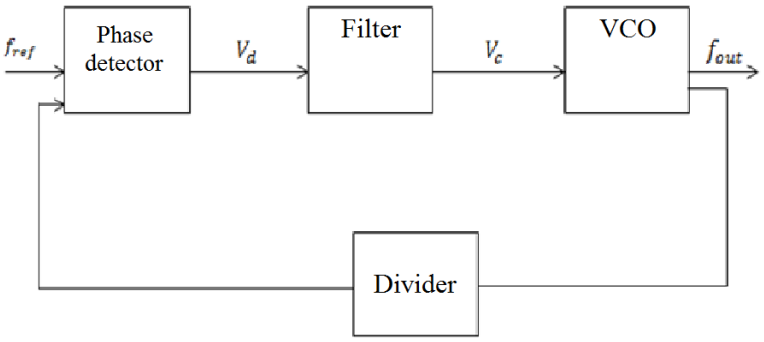


FIG. 2. Block scheme of a PLL synthesizer.

Figure 2. represents a block diagram of a PLL circuit. Initially we have input frequency, that is applied to the input of a phase detector.This generates a voltage outputV_d, whose average value is proportional with the phase difference signal from the detector inlet. The error signal of the phase detector appliess to the input of the loop

filter.This will generate a voltage proportional to the phase error voltage. This voltage control signal is voltage controlled oscillator OCT. In this way the frequency of the output signal f_{out} changes according to the existing momentary error.

GenerallyV$_d$ is:

$$V_d = f(\omega_{int} - \omega_{out}, \theta_{in} - \theta_{out}, \omega_{int} + \omega_{out}, \theta_{in} + \theta_{out}), \quad (3)$$

$$(V_c) = \frac{d\theta_{out}}{dt} \quad (4)$$

PLL architecture is one of the most used among frequency synthesizers because it can be easily integrated into XXI century technologies. One of the main advantages of this method is that it uses a low power consumption. Other advantages of this method are: low production cost, simplicity of construction and permit obtaining relatively fast switching speeds. These advantages make this method very used in a wide range of communications from the audio to the one of the millimeter-wave . PLL method is widely used in wireless communications through its architecture ΔΣ-PLL or fractional-N-method.

The major disadvantage of this method is that it is difficult to obtain digital modulation type and is also difficult to obtain high resolution. Also, good quality oscillators are quite expensive and very bulky leading to restrict their use in a wide variety of communications field such as mobile phones or laptops.

DDS Digital Direct Method

The main elements of the architecture of a direct digital frequency synthesizer are: phase battery, memory, or conversion device using phase-amplitude sine function and digital-to-analog converter. Each of these elements can lead to distort the spectral components of the output signal spectral structure.

At higher operating frequencies, another source of noise consists of transitions that occur when switching from one state to another.

Reduced switching time is required in applications such as frequency hopping radio systems. From this point of view, direct digital synthesis method offers outstanding performance.

DDS architecture out of a battery is related to the entry phase by the following equation:

$$f_{out} = \frac{K}{2^N} \cdot f_{clk}, \quad (5)$$

where N is the length of the arm of a battery, the battery K is the value entry,and frequency control is ff_{clk}. Output frequency range is limited by f_{clk}, thus the maximum output cannot be greater than 400 MHz due to technological limitations.

The total number of possible phases is2^L (L- accumulator size in bits register).

By definition we have:

$2^L=2\pi$ (6)

L represent spread network frequency output achieved.

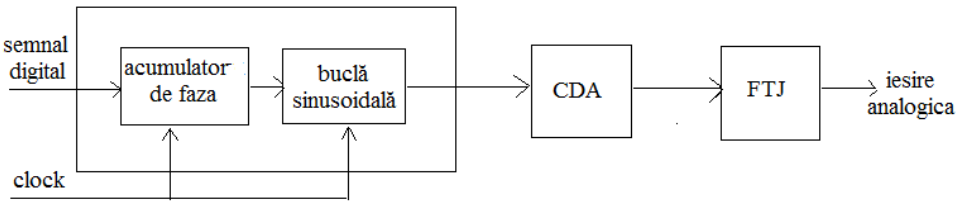


FIG.3 Direct digital synthesis block diagram.

It is shown in Fig.3.block diagram of a synthesizer that uses DDS frequency synthesis method. In the figure above are presented the main elements of an architecture of this kind, namely battery-digital converter and analog sine loop and a low pass filter for filtering signal. The main block is inserted the digital signal so that these enter into Converter. It can have a function sine, cosine, or both. On leaving the furnace signal is filtered by a low pass filter (to improve signal output) following to get the analog signal.

Synthesizers that are based on DDS direct method are used in the Army because it offers many advantages to the military, one of them would be the possibility of implementing any type of modulation. This is possible because it always knows phase, frequency and amplitude of a signal. Also, this method facilitates working in frequency hopping affords great carts, saving network frequencies, rapid scanning of the network, dial a synthesized frequency network, good or very good performance for the unwanted components output.

Also, this method has some less good parts, like for example that the circuits operate at maximum f_{clk}, which means a high energy consumption. Also, a disadvantage of this synthesis is the performance limiting of the digital-to-analog converter, or the occurrence of unwanted spectral components from the effects of truncation, in particular the phase truncation and the operation of the digital-to-analog converter.

Truncates of the bit length value sin (θ) (denoted by W) are stored in memory. The length of the sample phase bits (denoted by D) leads to the appearance of unwanted spectral components in the structure the signal output.

Sizes D and W contribute to increased quantization noise. Signal to noise ratio SNR (Signal Noise Ratio) at a frequency synthesizer can be calculated with the following formula:

$SNR_t = 2^w \cdot \frac{1}{2\pi^2}$, sau în decibeli: $SNR_t(dB) = (6W\text{-}13)\ dB$ (7)

Following the continuity phase generated signal, digital direct synthesis results in performance for digital modulations FSK, QPAK, BPSK, MSK, GMSK, which is impossible with other synthesis methods.

Direct synthesis allows to obtain phase modulation with outstanding frequency performance on precision.

3 ANALYSING THE BEHAVIOR OF A FREQUENCY SYNTHESIZER

For early analysis I selected block diagram of a PLL synthesizer, which is in the figure below.

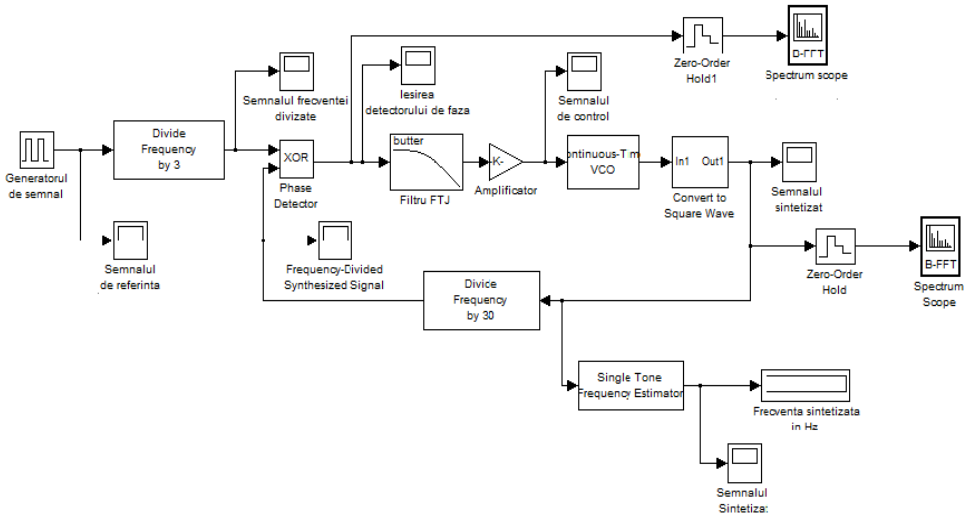
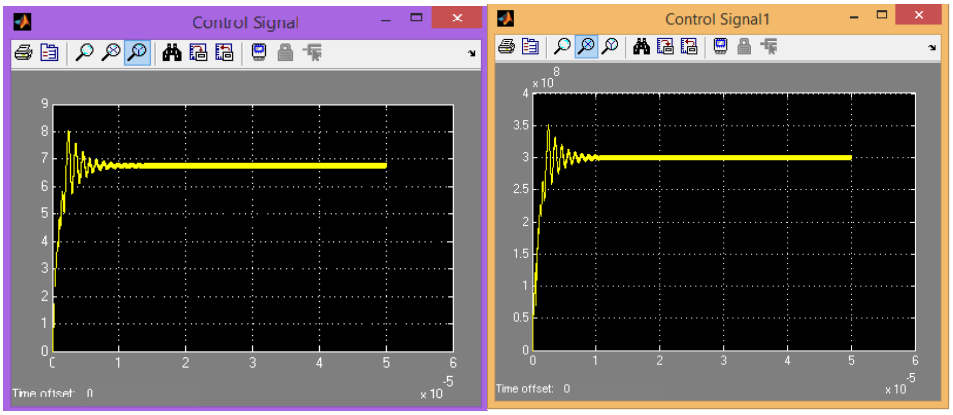


FIG.4. A PLL frequency synthesizer scheme in Simulink.

Figure 4 represents the block diagram of a frequency synthesizer with PLL phase horseback. The reference signal is obtained from the digital signal generator. M frequency divider, divides the frequency reference by m times, after which the signal enters the loop timing.The phase detector apply logical operation "or" to both reference and synthesized divided frequency .The filter is low pass and ensure the voltage needed to trigger the controlled oscillator voltage (with amplifier).It also filters high frequencies. The signal is amplified by an amplifier withconstant size at the output. Voltage controlled oscillator controls the frequency synthesized signal through control signal input. This concerns the output signal of synthesizer.*Voltage controlled oscillator with digital analog converter generates the synthesized signal.*

Value of output signal

$$f_{out} = 10MHz \times 30 \rightarrow \quad f_{out} = 300\ MHz \tag{8}$$



(a) (b)

In the Fig. a it can be seen the control signal that OCT's block receives the input signal frequency to maintain synthesized. This signal fluctuates initially for 10μs, following then to stabilize at constant value of 7/4. This happens when the model reaches an equilibrium.Fig. b is output from the PLL synthesizer. It can be seen that the signal has approximate the same features as the control signal acting OCT site. After amplifying, the signal fluctuates uncontrollably for about 10μs and then stabilizes at the desired frequency of 300 MHz. This synthesizer has a very good stability, an improvement that

can be added to it as time synchronization. The improvement can be done by adding a DDS structure as a reference signal for PLL synthesizer. DDS synthesizer uses the same principle as an NCO. The clock signal has a value of 100 MHz which makes value during sampling be 10^{-8}. Phase accumulator is offering sinusoidal input for signal loop. The accumulator is based on a function mode (mode) totaling values displayed between -1 and 1, and the values which exceed the range of -1 and 1 are not taken into consideration.

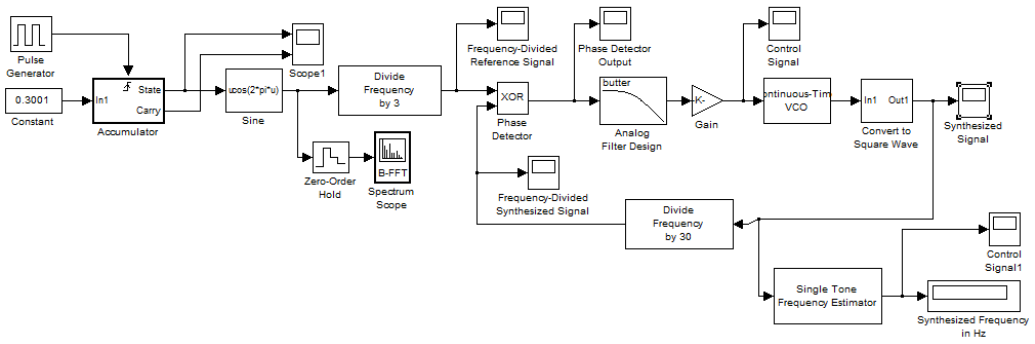
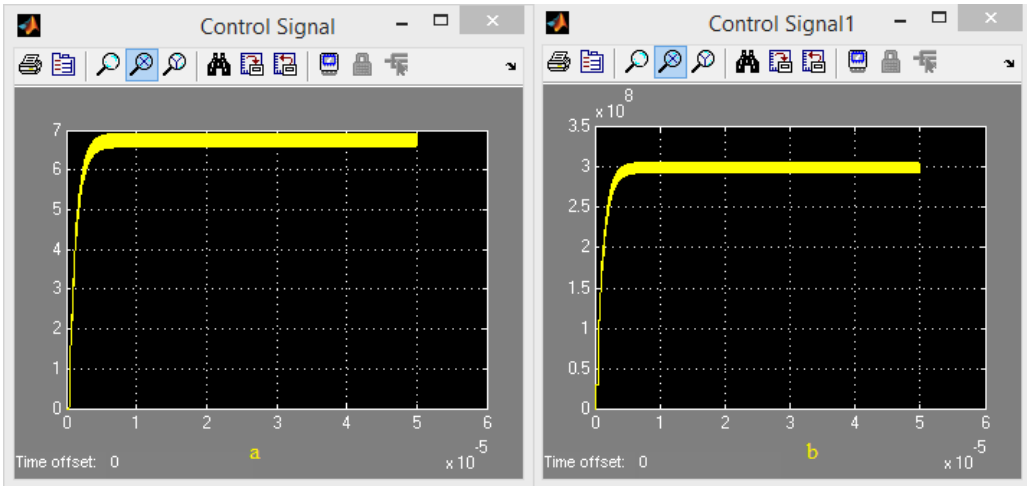


FIG.5.A hybrid frequency synthesizer scheme in Simulink..



(a) (b)

The amplification of signal at hybrid synthesizer is more direct, which makes the fluctuation to be much smaller, and the time it needs to stabilize is 5μs, instead of 10μs to the PLL synthesizer. Output frequency synthesizer has same value as in the previous section, namely 310 MHz. There is also a little difference for this value in favor of hybrid synthesis by the fact that the calculated value for simulator in PLL synthesizer is 295 MHz.

4. CONCLUSION

Considering all the requirements imposed by choosing this theme and considering everything that was caught during the development of this studywe can say that we presented the main methods of frequency synthesis used in communications, noting and brief analysis of one of the most common methods of frequency synthesizing and, not least, an analysis of a hybrid synthesizer.

We also demonstrated the operation of a PLL frequency synthesizer and how it can generate from any referencefrequency one or more frequencies of any order, and improving that kind of synthesizers by forming a hybrid frequency synthesizer. These ones are much better in terms of the time we live in,by the fact that it provides a much better stability compared with one PLL.

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