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TIMING COMPUTING IN ASYNCHRONOUS DIGITAL AUTOMATA

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Abstract: *In present paper, the authors has proposed a new idea for synthesis of an asynchronous digital system, using locally clock method . Driving an asynchronous digital system is much complex than a synchronous one. The authors has proposed a new method for synthesis of an asynchronous digital system using Verilog HDL Hardware Description Language, and also, the implementation into FPGA (Field Programable Gate Arrays) devices, [1-4]. The proposed method presented in this paper has many features like: execution speed much better, maximize the combinational/sequential digital logic, maximize the design performances (speed, low power, size).The CK and the output signals must be free of logic hazard;The minimum propagation delay of CK signal through the digital combinational system must be greater than the maximum propagation delay for every logic circuit which implements the input/output signals. Once the CK signal is triggered it can be reseted without digital hazard. Using the improved design described above, the entire asynchronous digital system will work with work correctly.*

Keywords: *Digital logic, FSM, Verilog HDL, Transition Table, ModelSim, Timing computations.*

1. INTRODUCTION

Driving an asynchronous digital system is a such complex task instead synchronous systems. The authors propose a method for synthesis of the asynchronous digital systems using Verilog HDL, and implement them into a FPGA devices, [1,2,3]. The proposed method presented in this paper has many features like:

- execution speed much better;
- maximize the combinational/sequential digital logic
- maximize the design performances (speed, low power, size)

A such of system is presented in figure 1. It contains the combinational logic modules, D type latches, input signals named input1,input2...inputN, output signals named output1,output2.....outputM, state variables named s1,s2...sk. The combinational system which implements an internal drive in signal, it is used for control the states of the digital system, disposal the hazard phenomenon from the digital systems. The entire system transit into a new state driving by the input signals which need to be stabile a period of time before changed and by the present states of the system.

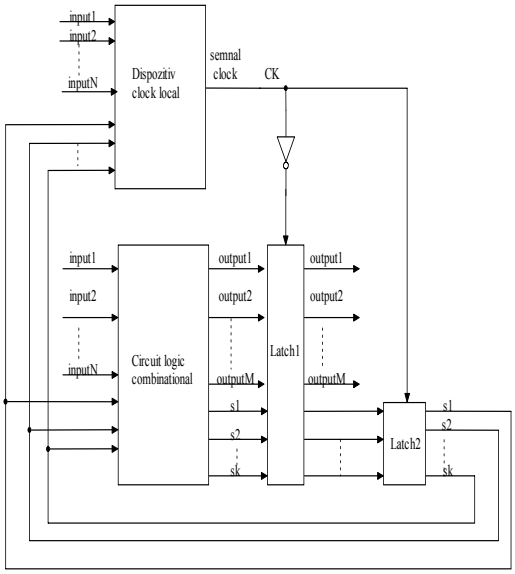

Fig.1. Digital Asynchronous System

In figure 1 it's shown the consist modules of the digital system:

- drive in signal device;
- combinational system who implements the system states equation ;
- D type latch1, latch2 are used to memorise the state of the system and also the outputs of the system;

The drive in signal (1) depends by the system's states notated with Q_i, input signals notated with X_j, where i=1,2,…n-1, j=1,2,…m-1; (n- states number variables, m-input number variables).

$$CK = F(Q_i, X_j) \qquad (1)$$

If signal CK=1 the system will go onto a new state, if CK=0 the system will stay in present state, it will can read the output values signals. While the states and outpus signals are computed, the input signals will not be changed, the system will work in fundamental mode.

2. DESIGN OF ASYNCHRONOUS DIGITAL SYSTEM WITH LOCALLY CLOCK METHOD

Let's consider an asynchronous digital system with functionality described by the fluence graph, figure 2:

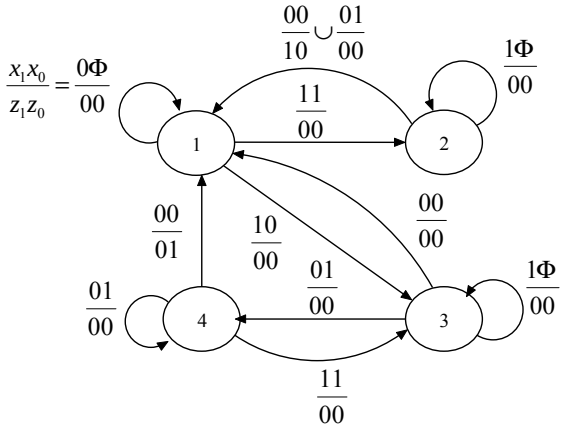

Figure 2. Graph table

The fluence table is described in figure 3.

Q_{n+1}/z_1z_0

$(x_1x_0)_n$ / Q_n	00	01	11	10
1	1/00	1/00	2/00	3/00
2	1/10	1/00	2/00	2/00
3	1/00	4/00	3/00	3/00
4	1/01	4/00	3/00	-/--

Fig.3. Fluence graph table

The equations are like, (2):

$$D_1 = y_{1,n+1} = [y_1(x_0 + x_1) + \overline{y_0}x_1\overline{x_0}]_n$$
$$D_0 = y_{0,n+1} = x_{1,n}$$
$$z_{1,n} = (\overline{y_1}y_0\,\overline{x_1}\,\overline{x_0})_n \qquad (2)$$
$$z_{0,n} = (y_1\overline{y_0}\,\overline{x_0})_n$$

The CK truth table is deducted from fig.3, like in fig.4:

y_1y_0 / $(x_1x_0)_n$	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	1	0	1	-

Fig. 4. CK truth table

Using the Veitch-Karnaugh, method it will compute the CK's equation (3):

$$CK = \overline{x_1}y_0 + x_1\overline{y_0} + \overline{x_0}y_1\overline{y_0} \qquad (3)$$

The D flip-flop circuits are described in fig.5:

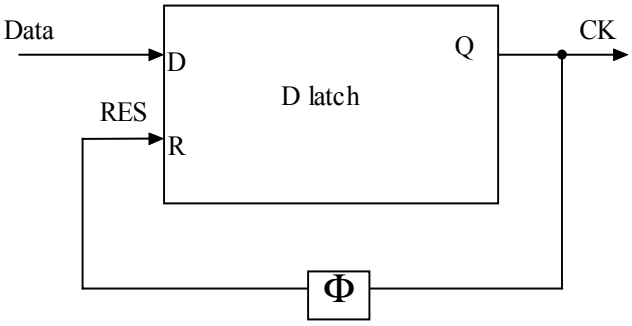

Fig.5. D flip-flop

z_1, z_0 - represents the outputs of the system
y_1, y_0 – represents the state of the system

The output signals z_1, z_0 and state signals y_1, y_0, has attached a D flil-flop latch. The D flip-flop latch1 stores the output signals while the latch2 stores the states signals. They are triggered on the positive clock signal – CK.
After a delay time, the CK signal is reseted who let the latch1 to be triggered.
The design of the proposed system is like in fig. 6.

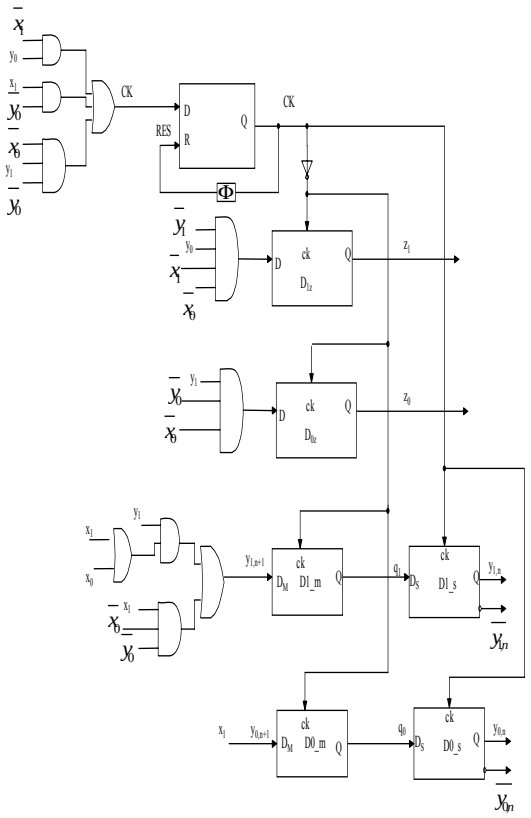

Fig 6. Design with D flip-flop

The entire digital system must meet the following restrictions:

- The minimum propagation delay of CK signal through the combinational system must be greater than the maximum propagation delay for every logic circuit which implements the input/output signals.

- Once the CK signal is triggered it can be reseted without digital hazard.

- Using the improved design described above, the entire asynchronous digital system will work concordant with the specifications.

- For a corect functionality, the following conditions must meet, fig.7.

$$\Phi << T$$
$$\Phi + \Delta = T$$
$$\Delta \le T$$
$$\Delta > \Phi$$

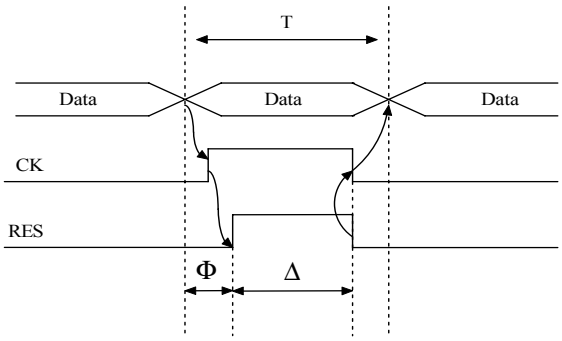

Fig 7. Functionality diagram

- If we set the value of delay time for the Q to Res signal $\Phi = 314ns$, we can use a RC circuit like:

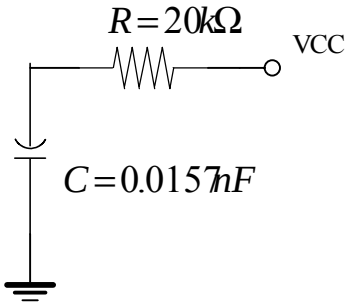

Fig. 8. RC circuit

Using the Fairchild Semiconductor Data Book, for the logic gates AND, OR, INV, D latch, can be deducted the following time requirements, fig.6:

Gate type	TP_{LH}	TP_{HL}
AND 2 inputs	7.6ns	8.8ns
AND 3 inputs	18ns	14ns
AND 4 inputs	7.6	8.8ns
OR 3 inputs	11.4ns	7.4ns
OR 2 inputs	10ns	14ns
D latch	8.5ns	13ns
Inverter	9.0ns	13ns

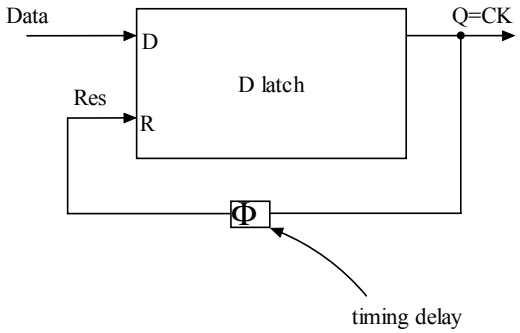

Figura 9. D latch logic cell

When TP_{LH} propagation time is taken into consideration, we have:

D_CK - the combinational digital logic implementation:

$$2 \cdot AND(2in) + 1 \cdot AND(3in) + 1 \cdot OR(3in) + 2 \cdot INV = \\ = 2 \cdot 7.6 + 1 \cdot 1.8 + 1 \cdot 11 + 2 \cdot 9 = 44.2 + 18 = 62.2ns \quad (4)$$

D_1 - the combinational digital logic implementation:

$$1 \cdot AND(4in) + 2 \cdot INV = 7.6 + 18 = 25.6ns \quad (5)$$

D_0 - the combinational digital logic implementation:

$$1 \cdot AND(3in) + 2 \cdot INV = 18 + 18 = 36ns \quad (6)$$

$y_{1,n+1}$- the combinational digital logic implementation:

$$1 \cdot AND(2in) + 2 \cdot OR(2in) + 3 \cdot AND(3in) + 1 \cdot INV = \\ = 1 \cdot 7.6 + 2 \cdot 10 + 3 \cdot 18 + 9 = 81.6 + 9 = 90.6ns \quad (7)$$

The Φ delay is compted with the next propagation delays,

$$\Phi = T_{p(D\_CK)} + T_{p(DI)} + T_{p(DO)} + T_{p(yl,n+1)} + T_{p(DIz)} + T_{p(DOz)} + T_{p(DI\_m)} + T_{p(DI\_s)} + T_{p(DO\_m)} + T_{p(DO\_s)} =$$
$$= 622 + 256 + 36 + 906 + 8.5 + 8.5 + 8.5 + 8.5 + 8.5 + 8.5 = 2654 ns \quad (8)$$

3. CONCLUSIONS

- The CK signal and the output signals must be free of logic hazard inorder to met the system run like within the specifications;

- The minimum propagation delay of CK signal through the combinational system must be greater than the maximum propagation delay for every logic circuit which implements the input/output signals.

- Once the CK signal is triggered it can be reseted without digital hazard.

- Using the improved design described above, the entire asynchronous digital system will work like in the specifications.

4. REFERENCES

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